REMARKS

Claims 1-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (U.S. Patent No. 5,568,437) in view of Hall et al. (U.S. Patent No. 6,128,758).

Claim 1 recites "a plurality of random access memory (RAM) blocks" and "a plurality of test modules, each being coupled to a corresponding one of the RAM blocks".

As described in Applicant's Response to the previous Office Action, Jamal fails to teach "a plurality of random access memory (RAM) blocks" and a corresponding "plurality of test modules" as recited by Claim 1. Also, as described in Applicant's Response to the previous Office Action, Applicant indicated the reasons why it would not be obvious to simply multiply the BIST circuit 100 and RAM block 84 taught by Jamal. In addition, Applicant's Response to the previous Office Action indicates the reasons why Jamal does not teach or suggest "a dedicated test bus coupled to each of the test modules" as recited by Claim 1. Applicant renews these arguments in the present Response.

The Examiner indicates that Hall et al. remedies the deficiencies of Jamal. Hall et al. teaches the use of plural RAM (i.e., constellation RAM 104e, Deinterleaver RAM 106b and Reed Solomon RAM 106c). Hall et al. further teach that a "module test mode" is used "for testing the configuration registers and RAMs within the modules of device 100." (Hall et al., Col. 7, lines 16-19.)

However, Hall et al. explicitly teaches that "Under the module test mode ... an external tester" is used to read and write the configuration registers and RAMs. (Hall et al., Col. 7, lines 29-38.) Thus (like Jamal), Hall et al. fail to teach "a plurality of test modules, each being coupled to

a corresponding one of the RAM blocks" as recited by Claim 1.

For the above-described reasons, Claim 1 is allowable over Jamal in view of Hall et al. Claims 2-9, which depend from Claim 1, are allowable over Jamal in view of Hall et al. for at least the same reasons as Claim 1.

Claims 10-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal and Hall et al. and further in view of Grider et al. (U.S. Patent No. 5,515,540).

Claim 10, which depends from Claim 1, is allowable over Jamal and Hall et al. for at least the same reasons as Claim 1. Grider et al. fail to remedy the deficiencies of Jamal and Hall et al. Thus, Claim 10 is allowable over Jamal and Hall et al. in view of Grider et al.

In addition, Claim 10 recites "wherein each of the RAM blocks has a capacity of 32 Kb or less".

The Examiner concludes that it would have been obvious to one by using a RAM with a limited capacity, because one of ordinary skill in the art would easier use the smaller RAM's capacity in order to achieve higher reliability.

However, as described in the specification as originally filed, RAM blocks having a capacity of 32 kb or less do not typically include associated BIST circuitry. (Specification, paragraph [0005].) As a result, RAM blocks of this size are typically not tested, or are tested with significant difficulty. (Specification, paragraph [0003].) Thus, contrary to the Examiner's assertion, it would not be obvious to use a plurality of RAM blocks "with a limited capacity" in combination with corresponding test modules. For this additional reason, Claim 10 is allowable over Jamal and Hall et al. in view of Grider et al.

Claim 11 recites "accessing the RAM blocks through a dedicated test bus during a test mode to test the functionality of the RAM blocks prior to normal operation of the chip". As described in Applicant's Response to the previous Office Action, Jamal and Grider et al. fail to teach or suggest a dedicated test bus as recited by Claim 11. Hall et al. teach "a modular reusable bus architecture" which supports "communications between the modules within the computer system in their normal operations" and "allows the same system bus to be re used in different operation modes", including "a test mode". (Hall et al., Col. 2, lines 22-38.) Thus, Hall et al. teach away from a "dedicated test bus" as recited by Claim 11.

For these reasons, Claim 11 is allowable over Jamal and Hall et al. in view of Grider et al.

Claims 12-19, which depend from Claim 11, are allowable over Jamal and Hall et al. in view of Grider et al. for at least the same reasons as Claim 11.

In addition, Claim 12 recites "accessing the RAM blocks through dedicated test modules coupled to the test bus". As described in Applicant's Response to the previous Office Action, Jamal fails to teach or suggest more than one BIST unit. As described above in connection with Claim 1, Hall et al., which teaches an external tester, also fails to teach "dedicated test modules". For these reasons, Jamal and Hall et al. fail to teach accessing RAM blocks through dedicated test modules as recited by Claim 12. Grider et al. does not remedy this deficiency of Claim 12. For this additional reason, Claim 12 is allowable over Jamal and Hall in view of Grider et al.

In addition, Claim 14 recites "coupling the pads to the system circuitry during normal operation of the chip; and coupling the pads to the test bus during the test mode."

As described in Applicant's Response to the previous Office Action, Jamal fails to teach or suggest the steps of coupling recited by Claim 14. Hall et al., which teaches away from a dedicated test bus, fails to remedy this deficiency of Jamal. For this additional reason, Claim 14 is allowable over Jamal and Hall et al. in view of Grider et al.

IDT-1616 SN: 09/887,913

CONCLUSION

Claims 1-19 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned.

Respectfully submitted,

E. Eric Hoffman
Reg. No. 38,186
Attorney for Applicant
BEVER, HOFFMAN & HARMS, LLP

Customer No.: 027158
Tel. No.: (925) 895-3545
Fax No.: (925) 371-8187

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